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Practical evaluation of an interleaved boost AC-DC converter with power factor correction for a solid-state transformer
Supplementary Material

This supplementary material provides the detailed design data, simulation parameters, control implementation, full schematics, and the measured DC-bench data supporting the main article. Hardware validation was performed on a DC input; the AC-dependent characterisation (power factor, THD, and closed-loop regulation) is identified as future work and summarised at the end.

Bill of materials

The complete component list is given below. Quantities shown are as ordered; per-board usage is six MBR10100G diodes (four bridge, two boost), two IPP048N12N3G MOSFETs, two 220 µH inductors, one 2200 µF capacitor, and the sensing, gate-drive, and protection components described in the article.

Bill of materials for the interleaved boost PFC converter

Qty	Manufacturer PN	Description
12	MBR10100G (onsemi)	Diode, Schottky, 100 V, 10 A, TO-220-2
10	IPP048N12N3GXKSA1 (Infineon)	MOSFET, N-channel, 120 V, 100 A, TO-220-3
2	UVZ1J222MHD (Nichicon)	Capacitor, aluminium, 2200 µF, 63 V, 20%, radial
4	1140-221K-RC (Bourns)	Inductor, 220 µH, 7.4 A, 50 mΩ, radial
2	4527 (Keystone)	Fuse holder, cartridge, 250 V, 5 A, PCB
10	0217005.HXP (Littelfuse)	Fuse, glass, 5 A, 250 VAC, 5×20 mm
2	B57235S0609M051 (TDK)	NTC inrush current limiter, 10 Ω, 4 A, 9.5 mm
3	UCC27524ADR (TI)	Gate driver, low-side, dual, 8-SOIC
6	INA180A1IDBVR (TI)	Current-sense amplifier, gain 20 V/V, SOT-23-5
6	WSL2512R0200FEA (Vishay Dale)	Resistor (shunt), 0.02 Ω, 1%, 1 W, 2512
1	LAUNCHXL-F2800137 (TI)	LaunchPad, TMS320F2800137 evaluation board
2	RC0805FR-0747KL (Yageo)	Resistor, 47 kΩ, 1%, 0805 (voltage sense)
2	RC0402FR-7W3K3L (Yageo)	Resistor, 3.3 kΩ, 1%, 0402 (voltage sense)
10	RC0805FR-0710RL (Yageo)	Resistor, 10 Ω, 1%, 0805 (gate)
20	C0805C104K5RACTU (KEMET)	Capacitor, ceramic, 0.1 µF, 50 V, X7R, 0805
6	282837-2 (TE)	Terminal block, 2-pos, 5.08 mm, PCB
2	7-146256-0 (TE)	Header, vertical, 40-pos, 2.54 mm
2	2-534206-0 (TE)	Receptacle, 40-pos, 2.54 mm, gold, PCB

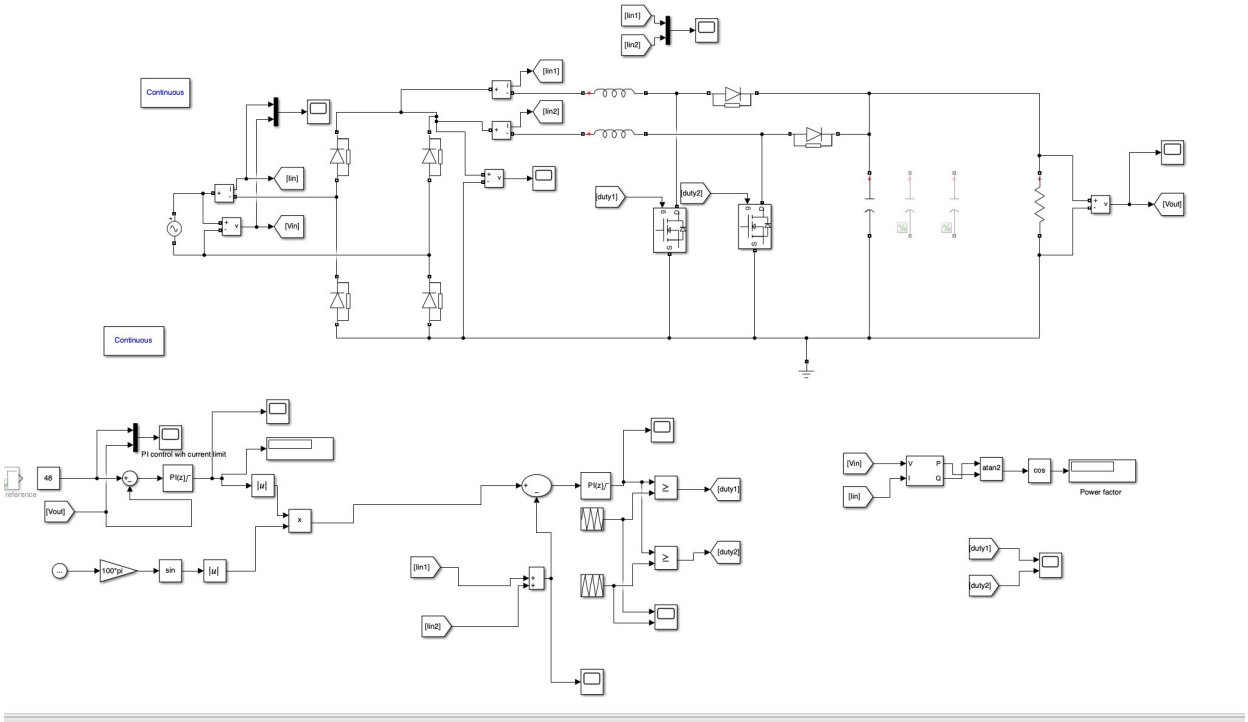
Design Equations and Sizing

The component-sizing equations are reproduced in the main article (equations 1—8). At the nominal operating point (24 V AC input, 48 V DC bus, 50 kHz, duty ≈ 0.29 at the rectified peak), the 220 µH boost inductors give a calculated per-leg peak-to-peak ripple of approximately 0.9 A, maintaining continuous conduction over the bulk of the line cycle, and the 2200 µF DC-link capacitor holds the simulated low-frequency (100 Hz) bus ripple to approximately 4.15 V peak-to-peak at full load. The output voltage divider (47 kΩ / 3.3 kΩ) scales the 48 V bus to approximately 3.15 V at the 3.3 V ADC input, and each 0.02 Ω

shunt with an INA180A1 (gain 20 V/V) produces approximately 0.4 V per ampere of leg current.

Simulation model parameters

Parameter	Value
Simulation platform	MATLAB/Simulink with Simscape Electrical
Solver	Fixed-step, 1 µs step (20 steps per switching period)
Controller discretisation	PI loops at 20 µs sample time, back-calculation anti-windup
Diode model	forward drop Vf = 0.8 V
MOSFET model	ideal switch (Vf = 0, no switching loss)
Inductor model	ideal (no series resistance)
Input source	24 V AC (rms), 50 Hz
Output voltage reference	48 V DC
Load	23 Ω resistive (~100 W)
Switching frequency	50 kHz
Boost inductance (per leg)	220 µH
DC-link capacitance	2200 µF
Carrier phase offset	180° between legs
Voltage loop PI	Kp = 0.1, Ki = 3, output limits [0, 7]
Current loop PI	Kp = 0.05, Ki = 3, output limits [0, 1]
Power-factor computation	from instantaneous P and Q (displacement factor)

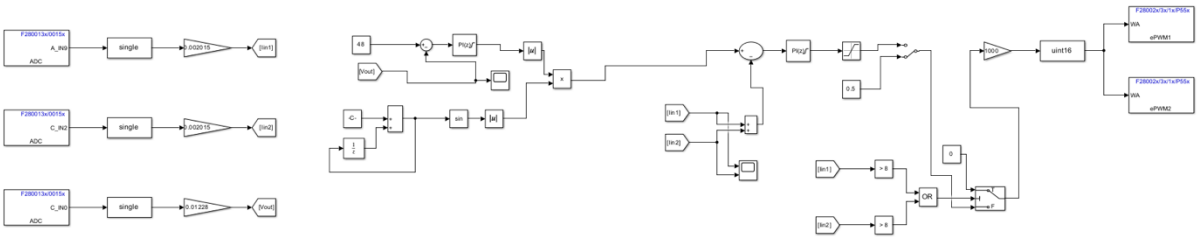


Complete MATLAB/Simulink model: power stage (top) and control system (bottom)

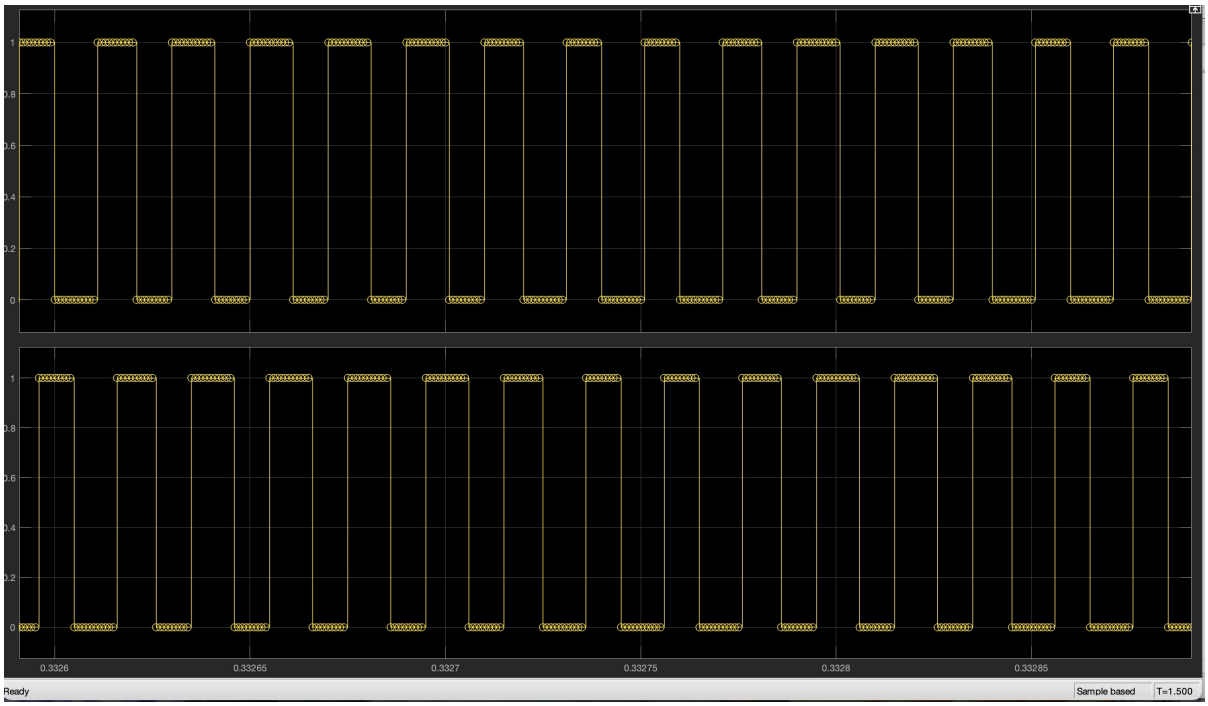
Digital control algorithm (Pseudocode)

The average-current-mode control is executed in a single interrupt service routine on the TMS320F2800137, synchronised to the 50 kHz PWM, as follows:

```
on each PWM/ADC interrupt (50 kHz):
    Vout = adc_Vout * k_v          // 47k/3.3k divider scaling
    IL   = (adc_IL1 + adc_IL2) * k_i   // summed leg current
    theta = input_phase()          // synchronised to rectified mains

    // outer voltage loop (PI, clamp 0..7)
    e_v  = VREF(48) - Vout
    Iamp = PI_voltage(e_v)         // Kp=0.1, Ki=3

    // shape current reference with rectified template
    Iref = Iamp * abs(sin(theta))

    // inner current loop (PI, clamp 0..1)
    e_i  = Iref - IL
    d    = PI_current(e_i)         // Kp=0.05, Ki=3

    // interleaved PWM output
    ePWM1.duty = d                 // carrier phase 0 deg
    ePWM2.duty = d                 // carrier phase 180 deg

    check_protection(OV, OC)       // over-voltage / over-current
```

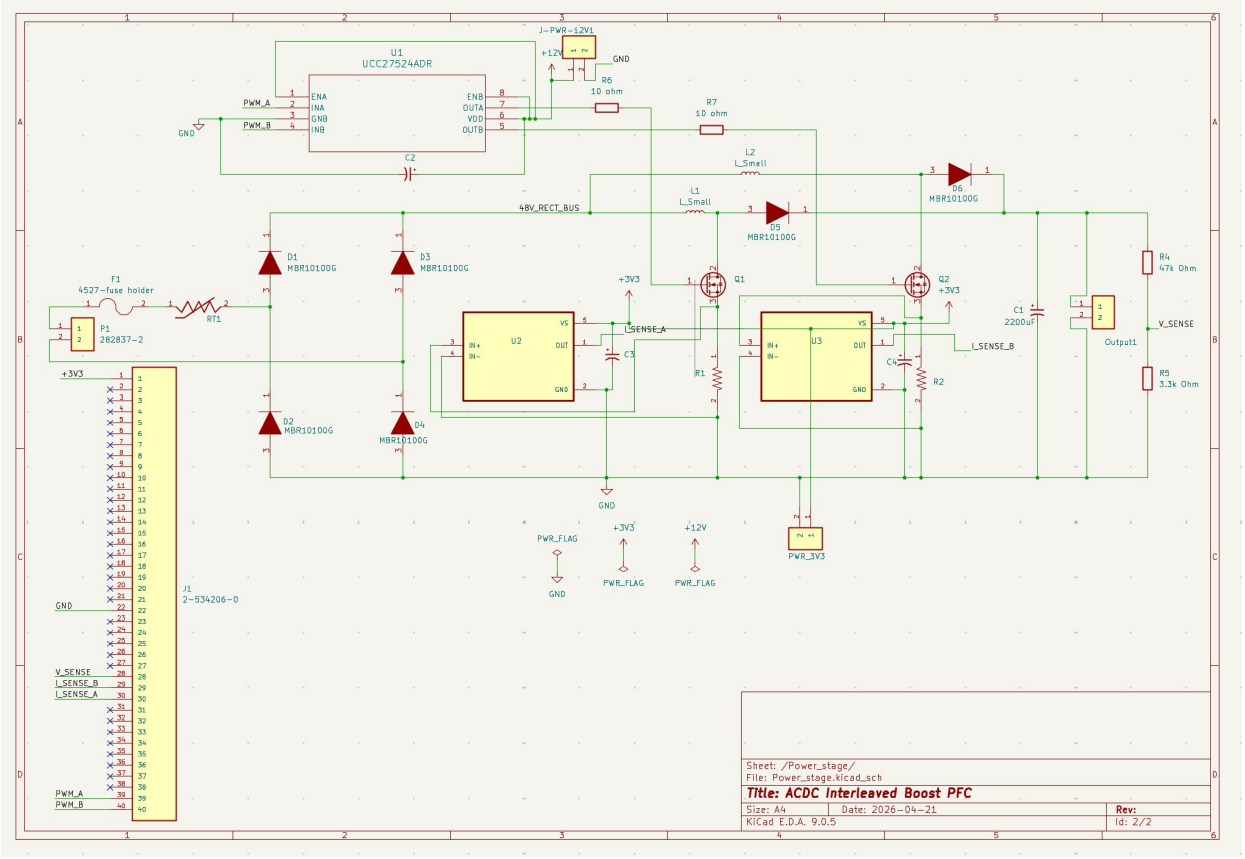


Hardware-target digital control implementation using the TI C2000 blockset, detailing ADC input scaling, average-current-mode PI loops, over-current protection, and ePWM generation



Gate-drive signals for the two legs (duty1 top, duty2 bottom), offset by approximately half a switching period (180° interleaving)

Power-stage schematic



KiCad power-stage schematic of the AC-DC interleaved boost PFC converter

Hardware Measurement Data (DC Bench)

The DC-bench campaign produced the measured data tabulated below. All values are DC operating points: Vin and Iin are read from the supply, Vout and Iout from the electronic load, with Pin = Vin·Iin, Pout = Vout·Iout, and efficiency = Pout/Pin. The current-sense outputs follow the 0.4 V/A scaling of the 0.02 Ω shunt and INA180A1 amplifier.

Clean DC rail with switching off (0% duty, no load): output equals input minus the bridge drop

Vin (V)	Vout (V)	Bridge drop (V)
5	4.367	0.63
10	9.28	0.72
15	14.21	0.79
20	19.16	0.84

Voltage-sense calibration: measured divider ratio against the 0.066 design value

Vout (V)	V_SENSE (V)	Ratio
9.28	0.608	0.0655
14.21	0.934	0.0657
19.16	1.257	0.0656

Open-loop boost duty sweep (10 V input, 0.5 A constant-current load): output tracks Vout ≈ Vin/(1−D)

Duty D	Vout (V)	Iin (A)	Pin (W)	Pout (W)	Eff (%)
0.10	8.294	0.55	5.50	4.15	75.4
0.20	9.156	0.61	6.10	4.58	75.0
0.30	10.232	0.68	6.80	5.12	75.2
0.40	11.551	0.77	7.70	5.78	75.0
0.50	13.265	0.88	8.80	6.63	75.4

Open-loop DC load sweep (20 V input, fixed 50% duty): efficiency peaks near 0.75 A

Iout (A)	Vin (V)	Iin (A)	Vout (V)	Pin (W)	Pout (W)	Eff (%)
0.25	20	0.58	38.22	11.60	9.56	82.4
0.50	20	0.91	30.65	18.20	15.33	84.2
0.75	20	1.34	30.53	26.80	22.90	85.4
1.00	20	1.78	30.29	35.60	30.29	85.1

Remaining for AC Characterisation (Future Work)

The following require a mains-frequency AC source and remain for future work: measured true power factor and input-current THD across the load range; closed-loop voltage regulation under AC input (not achievable on the DC bench because the power-factor current-shaping holds the average duty below the regulation point); the double-line-frequency (100 Hz) DC-bus ripple; and a current-probe measurement of the full inductor-current waveform to quantify the ripple-cancellation magnitude directly.